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EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,602	TANAKA ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5 and 8-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5 and 8-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
10/26/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/01/2006 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 4-5 and 8-18 have been considered but are moot in view of the new ground(s) of rejection. Currently, claims 2-3 and 6-7 are canceled and claims 1, 4-5 and 8-18 are pending for examination.

3. In response to applicant's argument regarding independent claim 1 rejected under 35 U.S.C. 103(a) that there is no suggestion to combine the references, as stated on page 10, 2nd paragraph. Applicant's argument has fully been considered, but is found not to be persuasive.

Please note that the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so

found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation is to increase the robustness of the interconnection between the disk array and the plurality of computer, because if one of the interconnection were to fail, another interconnection can be established (Pittelkow, col. 18, ll. 41-56).

4. In response to applicant's argument regarding dependent claim 4 rejected under 35 U.S.C. 103(a) that the combination of the references is improper as an additional interrupt signal line is required; and further more, there is no suggestion to combine the references, as stated on page 11, 3rd paragraph to 4th paragraph. Applicant's arguments have fully been considered, but are found not to be persuasive.

All three references are associated with the computer system, wherein the computer is coupled to the I/O device, and Stiffler and Pittelkow does not teach that by adding the additional interrupt line, the combined invention would become inoperable. Further more, the utilization of the interrupt signal is well known to one skilled in the art, as the utilization of the interrupt signal in the computer system would alleviate the burden of the computer to continually poll the I/O device.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 5 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "said control program" in page 3, ll. 16-18. There is insufficient antecedent basis for this limitation in the claim.

As per claim 5, it appear unclear which "said control program" the applicant is referring to. The examiner will examine claim 5 with the claimed limitation "said control program."

As per claim 8, claim 8 is rejected at least due to dependency on the rejected independent claim 5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 4-5, 8, 13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al. (US Patent 6,622,263) in view of Pittelkow et al. (US Patent 7,003,688).

7. As per claims 1 and 5, Stiffler teaches a computer system, comprising:

a plurality of physical partitioned computers (primary computer 601 and secondary computer 603 of Fig. 6) formed by partitioning a computer physically (Fig. 6);

an I/O device (Fig. 6, ref. 616) connected to a PCI bus (Fig. 6, ref. 610, 624) of said computer and shared among said plurality of physical partitioned computers (col. 9, l. 52 to col. 10, l. 10);

a port disposed in said I/O device and connected to said PCI bus (col. 9, ll. 52-56 and col. 10, ll. 3-7), wherein the disk array (i.e. I/O device) is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the I/O device would obviously have the single port; and

a PCI connection allocating means for setting a state of logical connection between selected one of said plurality of physical partitioned computers (primary computer 601 and secondary computer 603 of Fig. 6) and said port (Fig. 9 and col. 10, ll. 20-64); and

I/O device switching means for updating said state of connection set by said PCI connection allocating means according to a control signal received from said selected physical partitioned computer (Fig. 9 and col. 10, ll. 20-64), wherein the secondary computer implement the takeover control signal procedure,

wherein said selected physical partitioned computer (e.g. primary computer) changes its state of logical connection to said I/O device (e.g. disk array) according to the setting by said PCI connection allocating means (Fig. 6; Fig. 9 and col. 10, ll. 20-64), wherein the state of logical connection between the secondary computer and the disk array is changed by becoming active resulted form the takeover procedure, and the state of logical connection between the primary secondary and the disk array is deactivated as the primary computer is taken off-line,

wherein said selected physical partitioned computer (e.g. primary computer) is deactivated in response to occurrence to an error (e.g. in a fault state) in said selected physical partitioned computer (e.g. primary computer) (col. 10, ll. 20-64), as the take over procedure is implemented, the primary computer is deactivated by being taken off-line and the secondary computer take over the control of the disk array, and

a connection destination standby-system server (e.g. standby computer) becoming active resulted from the detection of the fault state (col. 14, ll. 35-63).

Stiffler does not expressly teach a computer system comprising:

wherein the port is a single port;

wherein the PCI connection allocating means for setting a state of logical connection between selected at most one of said plurality of physical partitioned computers and said port at a time; and

notification of the connection destination standby-system server of said state of connection.

Pittelkow teaches a system and method comprising

a storage assembly (Fig. 6, ref. 612) connected to a switch (Fig. 6, ref. 608) through a controller (Fig. 6, ref. 610), wherein a plurality of servers (Fig. 6, ref. 602, 604, 606) is coupled to the storage assembly through the switch, wherein said switch and controller enable at most one of said plurality of servers to be connected to the storage assembly at a time (col. 18, ll. 20-56); and

a configuration and control board for providing notification of failures (col. 8, ll. 49-52)

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Pittelkow's switch, controller and the notification of failure into Stiffler's computer system. The resulting combination of the references further teach:

said I/O device having the single port and is connected to said PCI bus, because the disk array (i.e. I/O device) is duplicated by having all disk stored initiated on the primary computer echoed by the second computer, therefore the disk array would obviously have the single port, which may be connected to a communication network to be accessible by both the primary computer and the secondary computer; and

having at most the secondary computer connected to the disk array at a time as the primary computer is taken off-line; and

notifying the standby computer (i.e. connection destination standby-system server) regarding the fault state as the primary computer is taken off-line and the standby computer becomes the active computer.

Therefore, it would have been obvious to combine Pittelkow with Stiffler for the benefit of increase the robustness of the interconnection between the disk array and the plurality of computer, because if one of the interconnection were to fail, another interconnection can be established (Pittelkow, col. 18, ll. 41-56).

8. As per claim 4 and 8, Stiffler and Pittelkow teach all the limitations of claims 1 and 5 as discussed above, where Stiffler further teaches the computer system comprising:

wherein first (Stiffler, primary computer 601 of Fig. 6) and second (Stiffler, secondary computer 603 of Fig. 6) physical partitioned computers are included in said plurality of physical partitioned computers (Stiffler, Fig. 6),

wherein said error detecting means, when detecting an error in said first physical partitioned computer (primary computer), sends a predetermined control signal to said I/O device switching means and connects said port of said I/O device to said second physical partitioned computer (Stiffler, col. 10, ll. 20-64), wherein the secondary computer detect the error with the primary computer and implement the takeover control signal procedure for the I/O device and connects to the I/O device operating as the primary computer, and

wherein said computer activates said second virtual machine and lets said first virtual machine stand by (Stiffler, col. 10, ll. 20-64), wherein the secondary computer become active and operating as the new primary computer while the failed primary computer is taken off-line.

9. As per claims 13 and 16, Stiffler teaches a method for sharing an I/O device (disk array 616 of Fig. 6) connected to a PCI bus (Fig. 6, ref. 610, 624) of a computer among a plurality of virtual machines (Fig. 6, ref. 601, 603) formed on a control program of said computer, comprising the steps of:

enabling said I/O device to set a state of logical connection between said selected virtual machine (primary computer 601 and secondary computer 603 of Fig. 6) (Fig. 6; Fig. 9 and col. 10, ll. 20-64) and a port of said I/O device connected to said PCI bus (Fig. 6, ref. 610, 624) through said port (col. 9, l. 52 to col. 10, l. 10), wherein the disk array is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the single port; and

changing said state of logical connection between said port and said selected virtual machine according to a control signal received from said selected virtual machine (Fig. 9 and col. 10, ll. 20-64), wherein upon implementing the takeover control signal procedure by the secondary computer, the logical connection between the primary computer and the disk array become deactivated as the primary computer is take off-line, and the logical connection between the disk array and the secondary computer becomes active and the secondary computer becomes the new primary computer.

Stiffler does not expressly teach the method comprising:

wherein the port is a single port; and

selecting at most one virtual machine among said plurality of virtual machines at a time.

Pittelkow teaches a system and method comprising

a storage assembly (Fig. 6, ref. 612) connected to a switch (Fig. 6, ref. 608) through a controller (Fig. 6, ref. 610), wherein a plurality of servers (Fig. 6, ref. 602, 604, 606) is coupled to the storage assembly through the switch, wherein said switch and controller enable at most one of said plurality of servers to be connected to the storage assembly at a time (col. 18, ll. 20-56).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Pittelkow's switch and controller into Stiffler's computer system. The resulting combination of the references further teach:

the I/O device's connection to the PCI bus utilizes the single port, because the disk array is duplicated by having all disk stored initiated on the primary computer echoed by the second computer, therefore the disk array would obviously have the single port, which may be connected to a communication network to be accessible by both the primary computer and the secondary computer; and

having at most the secondary computer connected to the disk array at a time as the primary computer is taken off-line.

Therefore, it would have been obvious to combine Pittelkow and Stiffler for reason stated above in claims 1 and 5.

10. As per claim 15, Stiffler and Pittelkow teach all the limitation of claim 13 as discussed above, where both further teach the method further comprising:

wherein said step of changing said state of logical connection, when detecting error occurrence in any of said plurality of virtual machines (e.g. primary computer), updates an allocation table for setting said state of logical connection between said port and each virtual machine, lets said error-detected virtual machine (e.g. primary computer) stand by (e.g. taken off-line) and activate another virtual machine (e.g. secondary computer) (Stiffler, col. 10, ll. 20-64 and col. 11, l. 51 to col. 12, l. 17 and Pittelkow col. 6, ll. 50-55), wherein when error occurrence is detected in the primary computer, the primary computer is taken off-line and the secondary computer is activated to become the new primary computer.

11. As per claim 17, Stiffler and Pittelkow teach all the limitation of claim 16 as discussed above, where both further teach the method further comprising:

wherein said step of changing said state of logical connection, when detecting error occurrence in any of said plurality of physical partitioned computers (e.g. primary computer 601 of Fig. 6), updates an allocation table for setting the state of logical connection between said port and each physical partitioned computer, lets said error-detected physical partitioned computer (e.g. primary computer) stand by (e.g. taken off-line), and activate another physical partitioned computer (e.g. secondary computer 603 of Fig. 6) (Stiffler, Fig. 6; Fig. 9; col. 10, ll. 20-49 and col. 11, l. 51 to col. 12, l. 17 and Pittelkow col. 6, ll. 50-55), wherein upon detection of the primary computer failed, the

primary computer is taken off-line and the secondary computer is activated to become the new primary computer.

12. Claims 9-12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al. (US Patent 6,622,263) in view of "Computer Input/Output".

13. As per claim 9, Stiffler teaches an I/O device (disk array 616 of Fig. 6) connected to a PCI bus of a computer (primary computer 601 and secondary computer 603 of Fig. 6), comprising:

a port connected to said PCI bus (Fig. 6 and col. 10, ll. 20-64), wherein the disk array is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the single port;

an operating system performing hot-add/remove an I/O device (disk array 616 of Fig. 6) (col. 14, ll. 54-58), wherein the hot-add/remove the I/O device is implemented as all user tasks continue to be executed with no lost of data or program continuity;

change the state of logical connection of said port according to a control signal received from said computer (Fig. 6 and col. 10, ll. 20-64), wherein when the secondary computer detect error with the primary computer, the secondary computer implement the takeover control signal procedure to change the state of logical connection between the primary computer and the disk array by having the primary computer taken off-line; and

wherein said computer changes its state of logical connection to said port (Fig. 6 and col. 10, ll. 20-64), wherein upon the secondary computer implementing the takeover control signal procedure, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer.

Stiffler does not expressly teach the I/O device connected to the PCI bus of the computer, comprising:

wherein the port is a single port;

signal generating means for generating an interruption signal used to change the state of logical connection of said port according to a control signal received from said computer;

the interrupt signal causes the hot-add/remove of the I/O device; and

when receiving said interruption signal said computer changes its state of logical connection to said port.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I/O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt signal into Stiffler's computer system. The resulting combination of the references teaches further comprising:

the PCI bus connecting to the single port, because the disk array is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the single port, which may be connected to a communication network to be accessible by both the primary computer and the secondary computer;

generation of the interrupt signal by the disk array when the disk array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer; and

the disk array (i.e. I/O device) is hot-removed from the primary computer in response to the primary computer receiving and running the interrupt signal.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler because not only is the utilization of interrupt signals within the computer system

well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

14. As per claim 10, Stiffler and "Computer Input/Output" teach all the limitations of claim 9 as discussed above, where both further teach that the system comprising:

wherein said computer includes first (Stiffler, secondary computer 601 of Fig. 6) and second (Stiffler, primary computer 603 of Fig. 6) virtual machines formed therein (Stiffler, Fig. 6),

wherein said signal generating means sends the interruption signal to said second virtual machine (e.g. primary computer) to change said state of logical connection of said port to said first virtual machine (e.g. secondary computer) according to a control signal received from said first virtual machine (e.g. secondary computer) (Stiffler, Fig. 6 and col. 10, ll. 20-64 and "Computer Input/Output", section 4), wherein upon the disk array receiving the takeover control signal procedure from secondary computer and generating the interrupt to disable communication with the primary computer as the secondary computer takeover the communication by becoming active and operating as the new primary computer.

15. As per claim 11, Stiffler and "Computer Input/Output" teach all the limitations of claim 9 as discussed above, where both further teach that the system comprising:

comprising an allocating mean for setting said state logical connection of said port (Stiffler, Fig. 6 and col. 10, ll. 20-64), wherein the state of logical connection

between the primary computer and the disk array is set to be deactivated and the state of logical connection between the secondary computer and the disk array is set to be activated.

wherein said signal generating means generates an interruption signal and updates said allocating means for setting said state of logical connection of said port (Stiffler, Fig. 6 and col. 10, ll. 20-64 and "Computer Input/Output", section 4), wherein the disk array generate the interrupt signal and update the state of logical connection between the primary computer and the disk array to be deactivated and update the state of logical connection between the secondary computer and the disk array to be activated.

16. As per claim 12, Stiffler teaches an I/O device (disk array 616 of Fig. 6) connected to a plurality of physical partitioned computers (Fig. 6, ref. 601, 603) through a PCI bus (Fig. 6, ref. 610, 624), comprising:

a port connected to said PCI bus (col. 9, l. 52 to col. 10, l. 10), wherein the disk array (i.e. I/O device) is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the single port;

changing the state of logical connection between said port to a first physical partitioned computer (e.g. secondary computer) according to a control signal (e.g. takeover control signal procedure) received from said first physical partitioned computer (e.g. secondary computer) included in said plurality of physical partitioned computers

(col. 10, ll. 20-64), wherein when the secondary computer generated the takeover control signal procedure, the state of logical connection between the disk array and the secondary computer is activated; and

an operating system performing hot-add/remove an I/O device (disk array 616 of Fig. 6) (col. 14, ll. 54-58), wherein the hot-add/remove the I/O device is implemented as all user tasks continue to be executed with no lost of data or program continuity;

Stiffler does not expressly teach the system comprising:

wherein the port is a single port;

signal generating means for sending an interruption signal to said second physical partitioned computer to change a state of logical connection of said port to a first physical partitioned computer according to a control signal received from said first physical partitioned computer included in said plurality of physical partitioned computers; and

the interrupt signal causes the hot-add/remove of the I/O device.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I/O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt signal into Stiffler's computer system. The resulting combination of the references teaches further comprising:

the PCI bus is connecting to the I/O device's single port, because the disk array (i.e. I/O device) is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the single port, which may be connected to a communication network to be accessible by both the primary computer and the secondary computer;

generation of the interrupt signal by the disk array when the disk array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer; and

the disk array (i.e. I/O device) is hot-removed from the primary computer in response to the primary computer receiving and running the interrupt signal.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler because not only is the utilization of interrupt signals within the computer system well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

17. As per claim 18, Stiffler teaches a method for sharing an I/O device (disk array 616 of Fig. 6) connected to a PCI bus (Fig. 6, ref. 610, 624) of a computer among a plurality of virtual machines (Fig. 6, ref. 601, 603), wherein said method comprising the steps of:

enabling said I/O device (e.g. disk array) connected to said PCI bus (Fig. 6, ref. 610, 624) through its port to change the state of logical connection of said port according to a control signal received from any selected one of said plurality of virtual machines (e.g. secondary computer); and a step of changing said state of logical connection between said port and said selected virtual machine (e.g. secondary computer) accordingly (Fig. 6; col. 9, l. 52 to col. 10, l. 10 and col. 10, ll. 20-64), wherein the disk array (i.e. I/O device) is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the single port; and wherein upon receiving the takeover control signal procedure from the secondary computer, the state of logical connection between the disk array and the primary computer is deactivated as the primary computer is taken off-line, and the state of logical connection between the disk array and the secondary computer is activated as the secondary computer commence to operate as the new primary computer; and

performing hot-add/remove an I/O device (disk array 616 of Fig. 6) (col. 14, ll. 54-58), wherein the hot-add/remove the I/O device is implemented as all user tasks continue to be executed with no lost of data or program continuity;

Stiffler does not expressly teaches the system comprising:

wherein the port is a single port;

a step of enabling said I/O device to generate an interruption signal used to change the state of logical connection; and a step of changing said state of logical connection between said port and said selected virtual machine according to said received interruption signal; and

the interrupt signal causes the hot-add/remove of the I/O device.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I/O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt signal into Stiffler's computer system. The resulting combination of the references further teaches:

the PCI bus is connecting to the I/O device's single port, because the disk array (i.e. I/O device) is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the

single port, which may be connected to a communication network to be accessible by both the primary computer and the secondary computer;

generation of the interrupt signal by the disk array when the disk array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer; and

the disk array (i.e. I/O device) is hot-removed from the primary computer in response to the primary computer receiving and running the interrupt signal.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler because not only is the utilization of interrupt signals within the computer system well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

18. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al. (US Patent 6,622,263) and Pittelkow et al. (US Patent 7,003,688), and further in view of "Computer Input/Output".

Stiffler and Pittelkow teach all the limitations of claim 13 as discussed above, where Stiffler further teaches the system comprising wherein said step of changing said state of logical connection includes a step of changing said state of logical connection

between said port and said selected virtual machine (Fig. 6 and col. 10, ll. 20-64), wherein the state of logical connection between the primary computer and the disk array is deactivated and the state of logical connection between the secondary computer and the disk array is activated.

Stiffler and Pittelkow does not teach the system comprising:

generating an interruption to notify said selected virtual machine of a change of said state of logical connection of said I/O device; and

a step of enabling said selected virtual machine that receives said interruption to change said state of logical connection to said I/O device according to said setting of said state of logical connection.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I/O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt signal into Stiffler and Pittelkow's computer system. The resulting combination of the references teaches further comprising generation of the interrupt signal by the disk array when the disk

array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler and Pittelkow because not only is the utilization of interrupt signals within the computer system well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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